PHCC−to−Host Protocol

T	T	T	S	S	X	X	X
MSB 7	6	5	4	3	2	1	0 LSB

first Byte

T Type
S Size/bytes to follow
X Payload

Table of Types:

T	Meaning
000	all−bits−zero byte
001	key matrix update
010	analog update
011	I2C
100	keymatrix full bitmap
101	analog all axes dump
110	[unused]
111	all−bits−one byte

The first Byte determines the interpretation of the following bytes, depending on Type.

All Packets (ie. consecutive bytes in a transmission that belong together) are terminated with an all bits zero byte

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Key Matrix Update Packet

0	0	1	0	1	A9	A8	A7
MSB 7	6	5	4	3	2	1	0 LSB

Byte 1

A6	A5	A4	A3	A2	A1	A0	S
MSB 7	6	5	4	3	2	1	0 LSB

Byte 2

Bytes−to−follow field (bits 3−4 of Byte 1) specifies that one (01 binary) Byte will follow to make up a packet.
A0−A9 specify the address of the switch/pushbutton/rotary/... in the keymatrix that has changed.
S is the new state of that position in the keymatrix. (1=on/0=off)

Analog Update Packet

0	1	0	1	0	A8	A7	A6
MSB 7	6	5	4	3	2	1	0 LSB

Byte 1

A6−A8 are for future expansion, currently not used (zero)

A5	A4	A3	A2	A1	A0	D9	D8
MSB 7	6	5	4	3	2	1	0 LSB

Byte 2

A0−A5 specify which analog channel

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 3

D0−D9 contains the 10−bit ADC result

I2C Raw Data Packet

0	1	1	1	0	xx	A9	A8
MSB 7	6	5	4	3	2	1	0 LSB

Byte 1

xx is unused field

A7	A6	A5	A4	A3	A2	A1	A0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 2

A0−A9 specify the I2C device address

D0−D9 contains the payload data from that I2C device

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 3

data format is application specific

Key Matrix Full Map Packet

1	0	0	/	/	/	/	/
MSB 7	6	5	4	3	2	1	0 LSB

Byte 1

b	b	b	b	b	b	b	b
MSB 7	6	5	4	3	2	1	0 LSB

Byte 2..129

bytes 2−129 are the bit map ofthe key matrix state
byte 2 contains switches 0−7,byte 3 contains switches 8−15,
byte 129 contains switches 1016−1023

1	1	1	1	1	1	1	1
MSB 7	6	5	4	3	2	1	0 LSB

Byte 130 "all−bits−one−byte"

0	0	0	0	0	0	0	0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 131 "all−bits−zero−byte"

Bytes 130 and 131 are the termination sequence for the Key Matrix Full Map Packet

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Analog All Axes Dump Packet

1	0	1	/	/	/	/	/
MSB 7	6	5	4	3	2	1	0 LSB

Byte 1

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 2 Lower 8 bits of ANP0

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 3 Lower 8 bits of ANP1

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 4 Lower 8 bits of ANP2

D7	D6	D5	D4	D3	D2	D1	D0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 5 Lower 8 bits of AN0

D9	D8	D9	D8	D9	D8	D9	D8
MSB 7	6	5	4	3	2	1	0 LSB
	AN0		ANP2		ANP1		ANP0

Byte 6 Upper 2 bits of ANP0, ANP1, ANP2, AN0

[...] repeat for AN1 to AN31 using this 4+1 scheme

1	1	1	1	1	1	1	1
MSB 7	6	5	4	3	2	1	0 LSB

Byte 47 "all−bits−one−byte"

0	0	0	0	0	0	0	0
MSB 7	6	5	4	3	2	1	0 LSB

Byte 48 "all−bits−zero−byte"

Bytes 47 and 48 are the termination sequence for the Key Matrix Full Map Packet