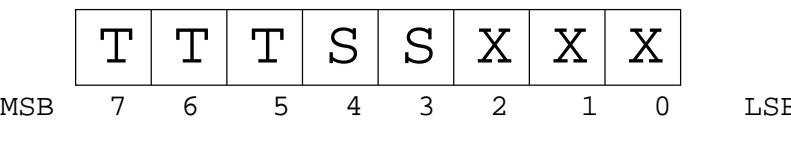


PHCC-to-Host Protocol



first Byte

T Type
S Size/bytes to follow
X Payload

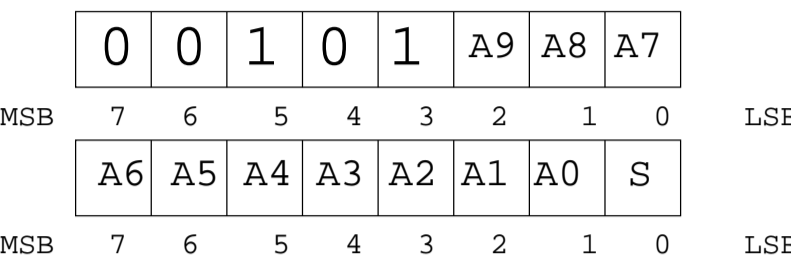
Table of Types:

T	Meaning
000	all-bits-zero byte
001	key matrix update
010	analog update
011	I2C
100	keymatrix full bitmap
101	analog all axes dump
110	[unused]
111	all-bits-one byte

The first Byte determines the interpretation of the following bytes, depending on Type.

All Packets (ie. consecutive bytes in a transmission that belong together) are terminated with an all bits zero byte

Key Matrix Update Packet

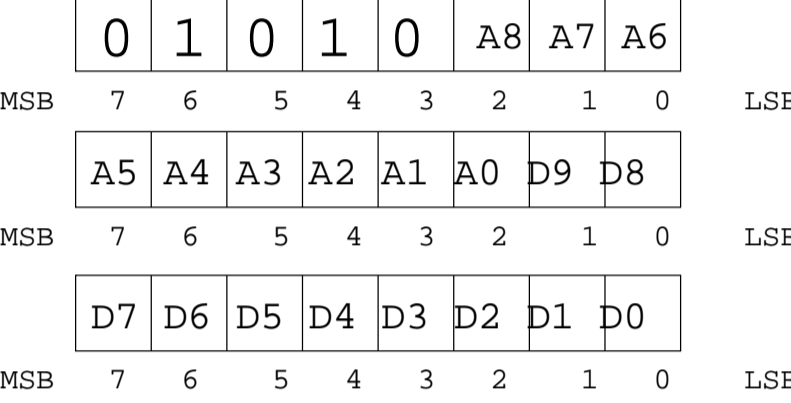


Byte 1

Byte 2

Bytes-to-follow field (bits 3-4 of Byte 1) specifies that one (01 binary) Byte will follow to make up a packet.
 A0-A9 specify the address of the switch/pushbutton/rotary/... in the keymatrix that has changed.
 S is the new state of that position in the keymatrix. (1=on/0=off)

Analog Update Packet



Byte 1

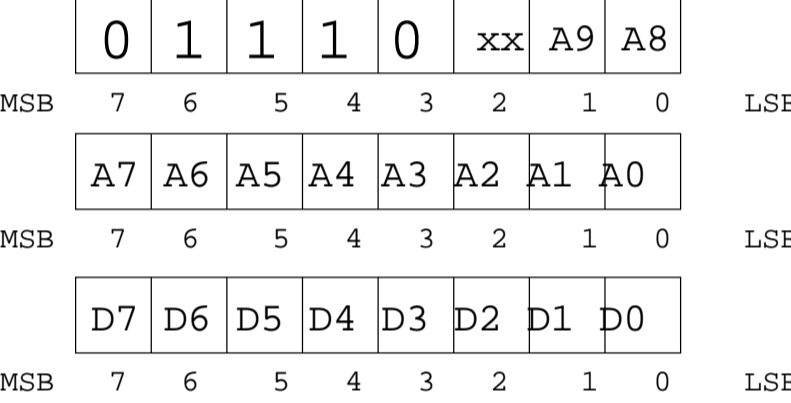
Byte 2

Byte 3

A6-A8 are for future expansion, currently not used (zero)

A0-A5 specify which analog channel
 D0-D9 contains the 10-bit ADC result

I2C Raw Data Packet



Byte 1

Byte 2

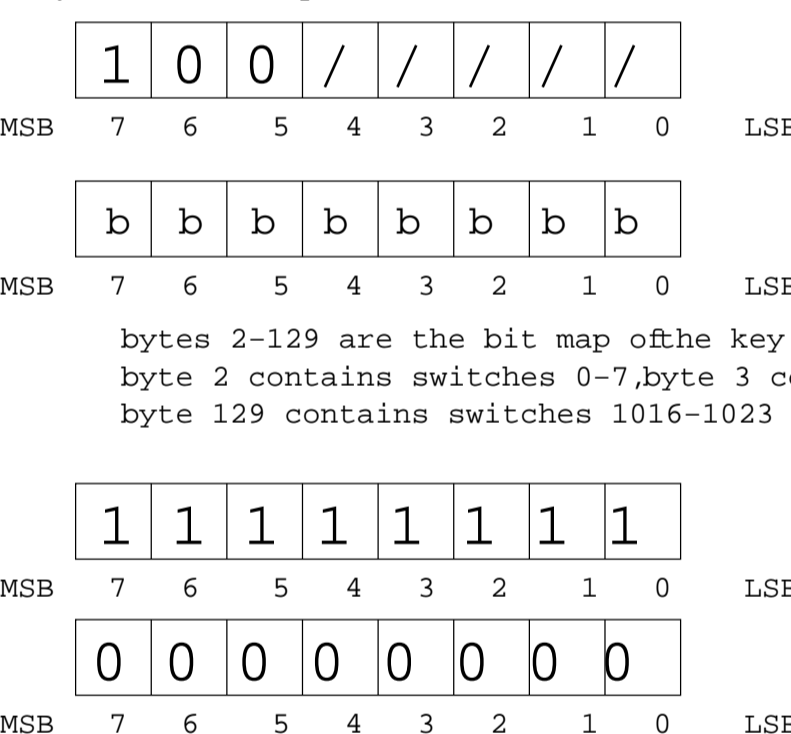
Byte 3

xx is unused field

A0-A9 specify the I2C device address

D0-D9 contains the payload data from that I2C device
 data format is application specific

Key Matrix Full Map Packet



Byte 1

Byte 2..129

Byte 130

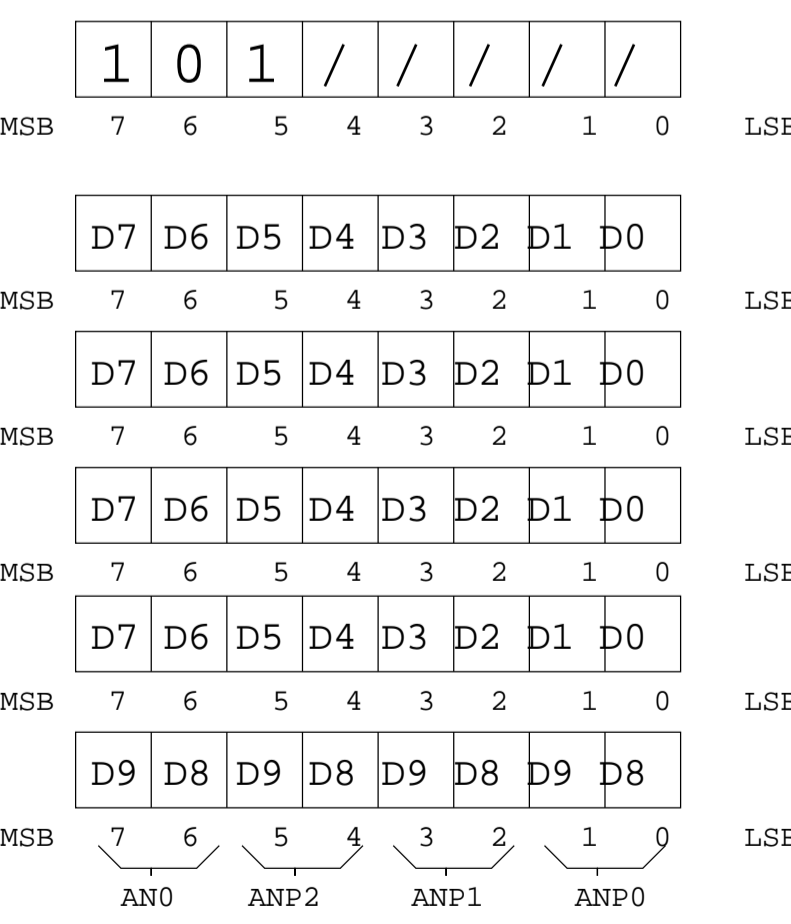
Byte 131

"all-bits-one-byte"

"all-bits-zero-byte"

Bytes 130 and 131 are the termination sequence for the Key Matrix Full Map Packet

Analog All Axes Dump Packet



Byte 1

Byte 2

Byte 3

Byte 4

Byte 5

Byte 6

Lower 8 bits of ANP0

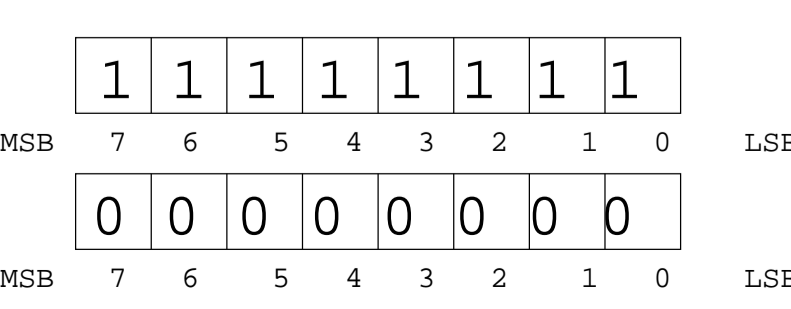
Lower 8 bits of ANP1

Lower 8 bits of ANP2

Lower 8 bits of AN0

Upper 2 bits of ANP0, ANP1, ANP2, AN0

[...] repeat for AN1 to AN31 using this 4+1 scheme



Byte 47

Byte 48

"all-bits-one-byte"

"all-bits-zero-byte"

Bytes 47 and 48 are the termination sequence for the Key Matrix Full Map Packet